ABSTRACT OF THE DISCLOSURE

When a communication speed of CPU 104 can be increased, a procedure of automatic phase adjustment involves setting phase shift amount CLK_DLY=n immediately after a vertical synchronization signal interrupt is generated, and reading video detection data VIDEO_DATA(n) after setting phase shift amount CLK_DLY=n+1 when the next vertical synchronization signal interrupt is generated. When CPU 104 is limited in the communication speed, the automatic adjustment is performed by an automatic adjusting circuit which has phase control data memory 107, video detection data memory 109, and a trigger input served by vertical synchronization signal S102.